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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,225	08/19/2003	Igor Keller	CA7017522001	6463

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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	**PAPER NUMBER**
2123	

MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,225	KELLER, IGOR	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 2/28/2007 has been received and fully considered.

2. Claims 24-41 are added; and now claims 1-41 are presented for examination.

3. Regarding the rejection under 35 USC 101, the Examiner withdraws the rejection in view of the amendment.

Response to Arguments

4.1 Applicant's arguments filed 02/28/2007 have been fully considered but are moot, in view of the new ground of rejection. However, in response to Applicant arguments that "Beakes fails to disclose or suggest determining slews of timing events, as recited in the present claims; and combining the arrival time of the timing input signal with any other timing parameter to determine worst case delay path or performance", the Examiner notes that the new grounds of rejections render moot these arguments, as a new reference is brought in to cover the amended version of the claims (*see below*).

4.2 While the applicant believes that the independent claims, along with the dependent claims should be found allowable, the examiner respectfully disagrees and asserts that the combined references cited teach the entire claimed invention. Applicant is further encouraged to look at the new references not used shown in the conclusion section below. However, the grounds of rejections below fully support the Examiner's position in rejecting the instant claims.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.0 Claims 1-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 6,430,731).

5.1 In considering the independent claims 1,6, 11, 19, 29, and 33, Lee et al. teaches Beakes et al. substantially teaches a method for determining a worst-case transition, and particularly teaches the steps of determining at least a plurality of different arrival times and different slews of timing events of based on a timing model of a gate *(col.2 lines16-33 and col.5 lines 1-5; also see col.7 lines 4-10)*; selecting a worst-case timing event from the plurality of timing events based on at least the combination of different arrival times and different slews of the timing events *(fig.11 col.7 lines 25-31 and col.14 lines 25-43; also see col.15 lines 44-48);* storing information related to the worst case timing event *(col.14 lines 40-43 and col.15 lines 52-62).*

5.2 As per claims 2,7, 12, and 20, Lee et al. teaches the step of determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate *(see Lee et al. col.4 lines 27-43*).

5.3 With regards to claims 3,8, 13, and 21, Lee et al. teaches that the step of selecting the worst-case input timing event further comprises the step of selecting a worst delay based on the gate delays *(see Lee et al. col.15 lines 44-48).*

5.4 Regarding claims 4,9, 14, and 22, Lee et al. teaches that the timing model comprises $To = Ti + Dg$, $Dg = F(S_I, C)$, $So = Q(S_I, C)$, where *To* is an output time, T_i is an input time, Dg is a gate delay, S_I is an input slew, C is a capacitive load of the gate, and *So* is an output slew, wherein the delay *Dg* of the gate depends, at least in part , on the slew of the input transition and capacitive load at the output of the gate (*see Lee et al. col.4 lines 27-43).*

5.5 Regarding claims 5,10, 15, and 23, Lee et al. teaches that the timing model is a timing library format (FTL) model (*see Lee et al. col.5 lines 7-17*).

5.6 With regards to claims 16-18, Lee et al. teaches that the output slews of the output timing events includes slew rate of the output timings, which is determined by an amount of time for a waveform to transition from a first voltage to a second voltage *(see Lee et al. col.2 lines 16-33).*

5.7 Regarding claim 24, Lee et al. teaches that the different arrival times comprise the arrival times of the timing event at each input of the gate *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43).*

5.8 As per claim 25, Lee et al. teaches that the different arrival times of the timing event at each input of the gate comprises the input times of the timing events *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43).*

5.9 With regards to claims 26,30, and 34, Lee et al. teaches that the different slews comprise transition times of the timing events through the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

5.10 Regarding claims 27,31, and 35, Lee et al. teaches that the transition times of the timing events through the gate are based on characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

5.11 As per claims 28,32, and 36, Lee et al. teaches that a duration of the transition times of the timing events through the gate is based on characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

5.12 With regards to claims 37-41, Lee et al. teaches that information related to the worst-case timing event is stored in a memory *(see Lee et al. col.14 lines 40-43 and col.15 lines 52-62).*

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6.1 Schultz (U.S. Patent No. 6,442,741) teaches a method of automatically generating schematic and waveform diagrams for analysis of timing margins and signal skews of relevant logic cells using input signal predictors and transition times.

6.2 Palermo (U.S. Patent No. 5,761,097) teaches a system and method for logic timing analysis for multiple-clock designs.

6.3 Chiu (U.S. Patent No. 7,047,508) teaches a method for performing multi-clock timing analysis.

7. Claims 1-41 are rejected and Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 4, 2007

APL

PAUL RODRIGUEZ
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